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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/640,369	08/13/2003	Raymond Bertram	CNTR.2200	8458

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/640,369	BERTRAM, RAYMOND	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6* is/are allowed.

6)☒ Claim(s) *7-9 and 12-17* is/are rejected.

7)☒ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 9, 12, and 17 are objected to because of the following informalities:

Claim 9, line 12, the recitation, "low" after pulled appears to be --high--. See Fig. 2B.

Claim 12, line 13, the recitation, "as" should be changed to --of-- in order to particularly point out and distinctly claim the subject matter.

Claim 17, line 5, the recitation, "second" appears to be --third--. See Fig. 2B and claim 7. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7 and 9 rejected under 35 U.S.C. 102(e) as being anticipated by Sprague et al. (US 6,496,038 B1, hereinafter, "Sprague").

Regarding claim 7, Sprague discloses, at least in Figs 2 and 3, a register comprising:

an evaluation circuit (210, 213, 235) that pre-charges a first node (237) while a clock signal (CK) is low and that evaluates a logic function for controlling the state of the first node when said clock signal goes high;

a storage circuit (250, 255, 275), coupled to said first node and receiving said clock signal, that drives a second node (267) high if said first node is low and that drives the second node low if said first node stays high when said clock signal goes high;

a keeper circuit (260, 265), coupled said second node, that drives (via 230A) a third node (output of 230A) to an inverted logic state (col. 8, lines 51+) as said second node; and

an output circuit (230B-230D), coupled to said first node (via 220) and said third node, that drives an output node high if said first or third nodes are low and that drives said output node low if said first and third nodes are both high.

Regarding claim 9, Sprague discloses, at least in Figs 2 and 3, that the storage circuit comprises:

a P-channel device (250), coupled to said first and second nodes, that pulls said second node high if said first node goes low;

a first N-channel device (255), coupled to said second node and receiving said clock signal; and

a second N-channel device (275), coupled to said first N-channel device and to said first node;

wherein said first and second N-channel devices collectively pull said second node low if said first node is pulled high in response to said clock signal going high.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Gayles et al. (US 6,191,618 B1, hereinafter, "Gayles").

Regarding claim 12, Gayles discloses, at least in Fig. 2, a method of registering a logic function and generating a non-inverted output signal, comprising:

pre-setting a first node (15) while a clock signal (CLK) is in a first logic state (LOW);

evaluating a logic function (12, 13) to control the logic state of the first node when the clock signal transitions to a second logic state (high);

driving a second node (output of 17) to an opposite logic state (LOW) of the first node in response to the clock signal transitioning to its second logic state;

maintaining (with 16 and 17) the second node at its previously driven logic state;

driving a third node (25) to an opposite logic state (high) of the second node; and

driving an output node (output of 27) based on the states of the first and third nodes (it can be based on the status of any preceding nodes).

Regarding claim 13, Gayles discloses, at least in Fig. 2, that said pre-setting a first node comprises pre-charging (11) the first node to a high logic state (when CLK=low).

Regarding claim 14, Gayles discloses, at least in Fig. 2, that said maintaining the second node at previously driven logic state comprises coupling a keeper circuit (16, 17) the second node.

Regarding claim 15, Gayles discloses, at least in Fig. 2, that said driving a second node comprises:

pulling the second node (output of 17) high if the first node (15) is low; and

pulling the second node (output of 17) low if the clock (CLK) and first nodes (15) are both high.

Regarding claim 16, Gayles discloses, at least in Fig. 2, that said driving a third node comprises inverting (D2) the state of the second node.

Regarding claim 17, Gayles discloses, at least in Fig. 2, that said driving an output node comprises:

pulling the output node (output of 27) high if either of the first (15)and third (25) nodes is low; and

pulling the output node low if the first (15) and third (25) nodes are both high.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7-9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ngo et al. (US 6,650,145 B2, "Ngo" hereinafter) in view of Sprague.

Regarding claim 7, Ngo discloses, in Fig. 2.1, a register comprising: an evaluation circuit (212, 204, 214) that pre-charges a first node (210) while a clock signal (CLOCK 224) is low and that evaluates a logic function for controlling the state of the first node when said clock signal goes high; a storage circuit (208, 206, 220), coupled to said first node and receiving said clock

signal, that drives a second node (228) high if said first node is low and that drives the second node low if said first node stays high when said clock signal goes high; a keeper circuit (226, 228), coupled said second node.

Ngo does not disclose an output circuit.

However, Sprague discloses an output circuit (230) in order to provide static logic stages (col. 8, lines 49+).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the dynamic logic circuit of Ngo with the output circuit as taught by Sprague in order to provide static logic stages at the end of dynamic logic circuit.

Regarding claim 8, Ngo discloses in Fig. 2.1, that said evaluation circuit comprises:

a P-channel device (212), coupled to said first node and receiving said clock signal, that pre-charges said first node while said clock signal is low;

a logic circuit (204), coupled to said first node, that evaluates said logic function based on at least one input data signal; and

an N-channel device (214), coupled said logic circuit and receiving said clock signal, that enables said logic circuit to evaluate said logic function when said clock signal goes high.

Regarding claim 9, Ngo discloses, at least in Fig. 2.1, that the storage circuit comprises:

a P-channel device (208), coupled to said first and second nodes, that pulls said second node high if said first node goes low;

a first N-channel device (206), coupled to said second node and receiving said clock signal; and

a second N-channel device (220), coupled to said first N-channel device and to said first node;

wherein said first and second N-channel devices collectively pull said second node low if said first node is pulled high in response to said clock signal going high.

Allowable Subject Matter

Claims 1-6 are allowed.

Claims 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER